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November 7, 2000

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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#3
1-11-01
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Subject:

Serial No. 09/654,776 09/05/00

C.T. Hsieh, D.S. Kuo, Y.F. Lin,
C.J. Lin, Jong Chen, H.D. Su

A METHOD TO INCREASE THE COUPLING
RATIO OF WORD LINE TO FLOATING GATE
BY LATERAL COUPLING IN STACKED-GATE
FLASH

Grp. Art Unit: 2822

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,480,821 to Chang, "Method of Fabricating
Source-Coupling, Split-Gate, Virtual Ground Flash EEPROM
Array", discloses a method of fabricating source-coupled
stacked-gate, virtual ground flash EEPROM array where a poly
floating gate of a cell is formed over a first portion of
channel region by a layer of floating gate oxide.

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U.S. Patent 5,412,238 to Chang, "Source-Coupling, Split-Gate, Virtual Ground Flash EEPROM Array", discloses a flash EEPROM array.

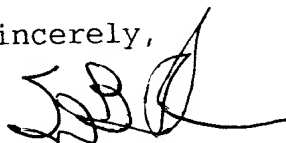
U.S. Patent 5,644,532 to Chang, "Method for Programming a Cell in a Source-Coupling, Split-Gate, Virtual Ground Flash EEPROM Array", discloses a method for programming a flash EEPROM array.

U.S. Patent 5,569,945 to Hong, "Stepped Floating Gate EPROM Device", discloses a stepped floating gate EEPROM device with a high coupling ratio.

U.S. Patent 5,686,333 to Sato, "Nonvolatile Semiconductor Memory Device and Method of Producing the Same", discloses a nonvolatile semiconductor memory device and a method of producing the same.

U.S. Patent 5,643,813 to Acocella et al., "Packing Density for Flash Memories by Using a Pad Oxide", discloses improved packing density as well as improved performance and higher manufacturing yields by confining floating gate structures between isolation structures covered with a thin nitride layer.

Sincerely,



Stephen B. Ackerman, Reg.# 37761